CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a first gate;

5 a second gate; and

source and drain regions adjacent and self-aligned to said first and second gate,

wherein said first gate and said source and drain regions are silicided in a single self-aligned process.

- 10 2. The integrated circuit in claim 1, further comprising a channel region between said first gate and said second gate.
 - 3. The integrated circuit in claim 1, further comprising conductors electrically connecting said first and said second gate.
 - 4. The integrated circuit in claim 1, further comprising an insulator above said first gate.

- 5. The integrated circuit in claim 2, further comprising insulators between said channel region and said first gate and said second gate.
- 6. The integrated circuit in claim 2, wherein said channel region includes channel extensions extending into said source and drain regions.
- 7. The integrated circuit in claim 6, wherein said channel extensions have an arrow shape in cross-section.
 - 8. A method of producing a double-gate metal oxide semiconductor field effect transistor comprising:

forming a laminated structure including a first sacrificial layer, a channel layer above said first sacrificial layer, and a second sacrificial layer above said channel layer; and

removing said first sacrificial layer and said second sacrificial layer; and depositing gate conductors around said at least two sides of said channel layer.

9. The method in claim 8, further comprising: doping source and drain regions of said laminated structure; and simultaneously siliciding said gate conductors and said source and drain regions using a self-aligned silicide process (salicide).

YOR9-2000-0173

10

- 10. The method in claim 9, wherein said doping immediatly precedes said siliciding.
- 11. The method in claim 8, further comprising forming an insulator between said channel layer and said first sacrificial layer and said second sacrificial layer.
- 5 12. The method in claim 8, further comprising forming conductors electrically connecting said gate conductors.
 - 13. The method in claim 8, further comprising:

 forming source and drain regions adjacent said laminated structure; and
 growing channel extensions into said source and drain regions.
- 10 14. The method in claim 12, wherein said channel extensions have an arrow shape in cross-section.
 - 15. The method in claim 8, wherein said removing of said first sacrificial layer and said second sacrificial layer leaves said channel layer as a bridge forming an open space above and below said channel layer.
- 15 16. A method of producing a double-gate metal oxide semiconductor field effect transistor comprising:

YOR9-2000-0173

forming a first sacrificial layer on a first surface of a channel layer;
forming a second sacrificial layer on a second surface of said channel
layer;

forming additional laminated layers on said first sacrificial layer and said second sacrificial layer to form a laminated structure;

removing said first sacrificial layer and said second sacrificial layer; and depositing gate conductors around said at least two sides of said channel layer.

17. The method in claim 16, further comprising:

doping source and drain regions of said laminated structure using a self-aligned process;

simultaneously siliciding said gate conductors and said source and drain regions using a self-aligned silicide process (salicide).

- 18. The method in claim 16, wherein said doping immediatly precedes said siliciding.
- 19. The method in claim 16, further comprising forming an insulator between said channel layer and said first sacrificial layer and said second sacrificial layer.

5

- 20. The method in claim 16, further comprising forming conductors electrically connecting said gate conductors.
- 21. The method in claim 16, further comprising:

 forming source and drain regions adjacent said laminated structure; and
 growing channel extensions into said source and drain regions.
 - 22. The method in claim 21, wherein said channel extensions have an arrow shape in cross-section.
- The method in claim 16, wherein said removing of said first sacrificial layer and said second sacrificial layer leaves said channel layer as a bridge
 forming an open space above and below said channel layer.